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YO998-426DIV



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of

Chan et al.

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filing Date: Concurrently Herewith

Examiner: Unknown

For: SELF-ALIGNED DOUBLE-GATE MOSFET BY SELECTIVE  
EPITAXY AND SILICON WAFER BONDING TECHNIQUES

Assistant Commissioner of Patents

Washington, D.C. 20231

**INFORMATION DISCLOSURE STATEMENT**

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicants' duty of disclosure under 37 CFR §1.56, applicants respectfully bring the following documents listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. All of these references were either cited or submitted in parent Application No. 09/272,297 and thus copies of these references are not provided in accordance with 37 C.F.R. §1.98(d).

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicants are aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

YO998-426DIV

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's  
Deposit Account No. 50-0510.

Respectfully submitted,



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